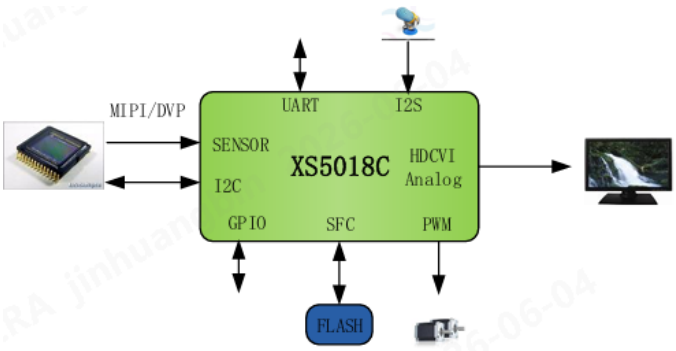
HIGH QUALITY CMOS ISP

5018C is a cost-effective image signal processing (ISP) chip designed for CMOS image sensors. It supports both MIPI and DVP interfaces and can connect to sensors up to 4M. It integrates a high-performance ISP processor with support for 3D noise reduction and digital wide dynamic range (WDR). For analog output, it supports 960H in standard definition, and HDCCTV 720P/1080P/4M in high definition. With a high level of integration for peripheral components, 5018C simplifies product design. It also embeds a CPU processor, enabling flexible software applications.

- **Built-in video Buffer and Comparator**
- **Supports HDcctv and CVBS**
- **960H/720P/1080P/4M**
- **High-performance 2D/3DNR**
- **Reduced Frame Rate**



- **Video input interface**
  - DVP@10bit
  - MIPI 2 Lanes
- **Peripheral**
  - POR
  - UARTx2
  - I2C x1
  - SPIx1
  - PWMx4
  - JTAG
  - Built-in comparator
  - Built-in High performance Video DAC and Buffer
- **ISP**
  - 2DNR
  - 3DNR
  - LSC
  - DPCC
  - GIC
  - CCM
  - AE、AWB
  - DWDR
  - Edge Enhanced process
  - Reduced Frame Rate
- **Camera Function**
  - Scaling and crop
  - Mask and OSD
- **DC Characteristics**
  - Core voltage: 1.1V
  - IO voltage: 3.3V
  - Sensor & I2C IO voltage: 1.8/3.3V
  - DAC/MIPI DPHY voltage: 3.3V
- **QFN7X7，68-pin，0.35mm pitch**
- **Video output**

  960H@25/30fps

  720P@25/30/50/60fps

  1080P@25/30fps

  4M@12.5/15/25/30fps

  5M@10/12.5/20/25fps