

AX615DV200 is an IPC SoC developed by Axera for module, channel, and consumer markets. Integrated with the cutting-edge AXProton 5.0 AI-ISP, this chip supports night vision of 5 M @ 30 fps. Its high-performance AXNeutron 5.0 NPU optimized for diverse scenarios makes AX615 to take a leading role in high-quality image processing and intelligent analysis. AX615 provides reliable and easy-to-use SDK, empowering you to mass produce

AX615DV200



Product Description

CPU

- Dual-core Cortex A7 1.0 GHz
- 32KB I-Cache
- 32 KB D-Cache
- Supports NEON acceleration
- Integrates FPU

NPU

- 2 TOPs
- Supports mixed precision
- Supports various mainstream deep learning frameworks

ISP

- Supports AI ISP up to 5 M @ 30 fps
- Supports 3A (AF, AWB, and AE)
- Supports image information statistics
- Supports AI-3DNR and 3DNR
- Supports AI-RLTM
- Supports 2-frame HDR
- Supports fixed pattern noise reduction
- Supports automatic detection and elimination of dynamic bad pixels
- Supports vignetting compensation
- Supports image enhancement
- Supports defogging function

Video Encoding

- H.264 HP/MP/BP Level 5.1 encoding
- H.265 MP Level 5.0 encoding
- Supports I/P frame for H.264/H.265 format
- Real-time multi-stream H.264/H.265 encoding capability: 5 Mp @ 30 fps + D1 @ 30 fps
- Supports bitrate control modes of CBR, VBR, AVBR, CVBR, FIXQP, and QMAP
- Supports encoding up to 8 ROIs
- JPEG snapping performance: 5 Mp @ 30 fps

Video and Image Processing

- Supports customizing the position and number of OSD overlays
- Supports mosaic
- Supports bitmap
- Supports video and image cropping

Hardware Interfaces

Video Interface

Input

- Supports 1 × 4 lane or 2 × 2 lane MIPI
- Supports up to 2.5 Gbps per lane

Output

- LCD 6/8 bit RGB or BT656
- Supports up to VGA or 5M BT output

Storage Interface

DDR interface

- SiP 1Gb
- Supports up to 2133Mbps

SPI Flash

- Supports SPI Nor Flash
- Supports SPI Nand Flash

eMMC Interface

- Supports eMMC v4.5

Peripheral Interface

Ethernet

- Supports 1-ch Ethernet port
- Supports TSO, UFO, and COE
- SiP RMII ePHY

USB

- Supports 1-ch USB 2.0
- Supports Host/Device mode

Other Interfaces

- SiP audio codec that supports I2S expansion
- Supports SDIO × 2, I2C × 3, SPI × 3, Uart × 3, PWM interfaces



WeChat Subscription Account



Official Website

Security

Built-in security module

- Supports secure boot
- Supports memory security isolation
- Hardware implementation of AES/DES/3DES encryption algorithms
- Hardware implementation of SHA-1, SHA-224, and SHA-256

Start-up

- Supports booting from eMMC
- Supports booting from SPI Nor Flash
- Supports booting from SPI Nand Flash

Physical Specs

Operating Voltage

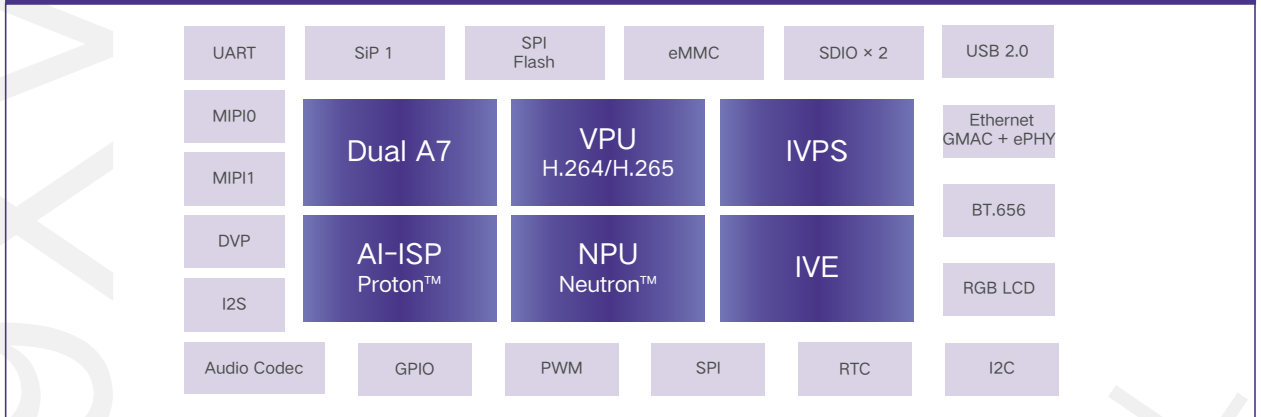
- Core voltage: 0.8 V
- DDR voltage: 1.35 V
- IO voltage: 1.8 V, 3.3 V

Packaging

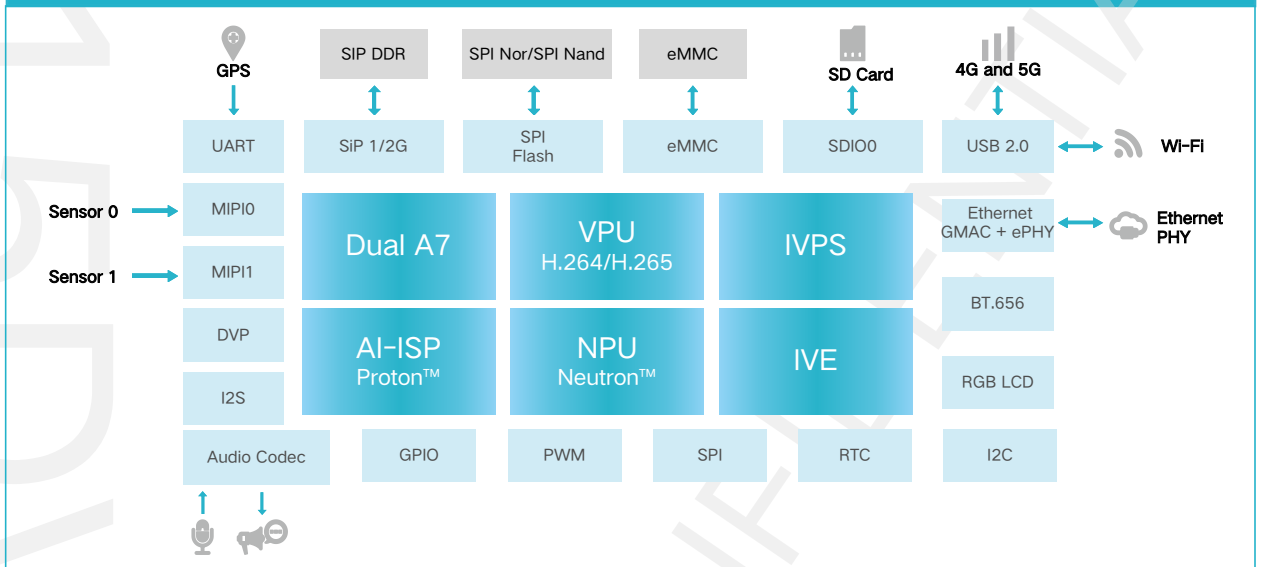
- QFN 10 × 10 mm

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AX615DV200 Product Diagram



Camera Solution for Industrial Applications



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